L1CTT RunIIb Upgrade System Review

July 29, 2005
Fermilab

This is a report on the D0 L1CTT RunIIb upgrade system review. The charge to the committee is included in the appendix. The purpose of this review was to assess the readiness of the L1CTT system for installation.

1 Details of the Review Process

The committee consisted of Marj Corcoran (Rice), Ken Johns (Arizona), Mike Matulik (Fermilab), and Brigitte Vachon (McGill). Ken Johns attended via video conference, and the other committee members were present in person. We met at 9AM CDT at Fermilab, in the D0 trailers. Also present were several managers: Vivian O'Dell (L1 manager), Paul Padley and Darien Wood (L2 managers) and Don Lincoln and Meenakshi Narain (Boston University) (L3 managers for the RunIIb CTT). The D0 Technical Coordinator, George Ginther, was also present. In the morning we heard presentations as outlined below. After the presentations we had a brief tour of the test setup in DAB3. We had a working lunch, and at 2:30PM we called back several people to ask questions. We adjourned around 4PM.

The agenda is included in the appendix. Vivian and Don gave brief introductory comments. Presentations were given by Eric Hazen (Boston University), Norik Khalatyan (Boston University, but resident at Fermilab), Samvel Khalatyan (also Boston University, but resident at Fermilab), and Stefan Gruenendahl(Fermilab). People present to provide additional information and answer questions were Jamieson Olson (Fermilab), Geoff Savage (Fermilab), and Shouxiang Wu (Boston). The review web page is

http://www-d0.fnal.gov/ lucifer/RunIIb/Welcome.html

which includes links to the slides presented.

2 Summary

All of the major parts of the L1CTT upgrade are complete and ready for installation. Having the system completed a few months before installation allows time for system-level tests. Several system tests have been performed with no serious problems discovered. We suggest additional tests which might be informative, but we did not feel that any of these tests were essential before installation.

3 Findings

The L1CTT upgrade is a system nearing completion. All of the major parts are in hand and tested. The system has undergone extensive testing both for the individual boards and for two fully-loaded crates. No serious problems have been found in the tests done so far. However, some additional testing should be done as detailed below.

3.1 Scope of the upgrade

The upgrade includes replacing the Digital Front End (DFEA) boards with an improved version, the DFEA2. The upgrade also entails removing the two DFE crates, and replacing them with crates which have most of the cabling in the back rather than the front. Much of the communication previously done through the front panels will be done through the backplane for the new system. This improvement will result in a cleaner and more stable cable plant. It also allows the addition of diagnostic front panel LEDs and direct access to the FPGAs, which will provide better debugging and testing capability. The original DFEA cards supplied a fast signal to the L1muon trigger. This functionality is retained, and in the new system a parallel signal is provided to the L1caltrack trigger. Figure 1 shows a block diagram of the CTT, but the additional link to L1caltrack is not shown.

The scope of the upgrade also includes a new crate controller and low voltage power supply distribution. The new crate controller will greatly increase the speed of firmware downloads, which was previously a serious bottleneck. The new low voltage power distribution uses three parallel 48V supplies with DC-to-DC converters on the DFEA2 boards. The new system has one redundant power supply on the platform as well as the ability to perform a hot swap. This is a great advantage in that the failure of one out of three power supplies will not bring down the system.

As part of re-doing crates and cabling, there may be some additional rearrangement of crates, but the details are not yet finalized.

The main improvement in the triggering algorithm consists of basing the tracks on CFT singlets rather than doublets as was done previously. This change increases the number of track equations by about a factor of 6, but it maintains high efficiency while increasing the rejection power about a factor of 10. Improvements in FPGAs over the past several years make the increased equation set manageable. The Xilinx chips used in the DFEA2 are a factor of 10 larger than than the previous chips, but there are only two per sector rather than four. The chips are expected to be only about 50% utilized, with the same safety factor in the RAM.

3.2 Current Status and Tests

The construction and initial testing of the DFEA2 boards has been done at Boston University. A total of 57 DFEA2 boards have been made, while only 40 are needed. A total of 49 boards were sent to Fermilab, of which three did not pass tests and were sent back to Boston. Of the three sent back, two appear to be working when tested again at BU, so their failure at Fermilab is a bit mysterious. Nevertheless, there appear to be adequate working and spare DFEA2 boards.

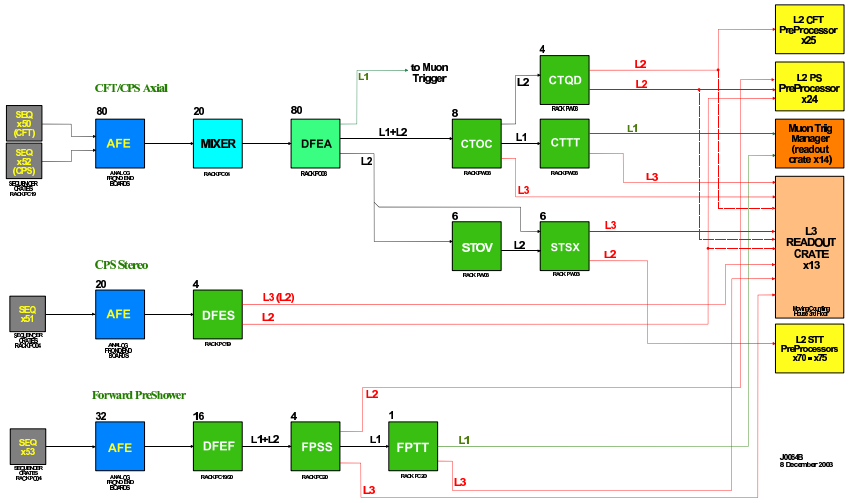

Figure 1: CTT block diagram. In this diagram, only the DFEA board is being replaced. In addition to the connection from the DFEA to L1muon, the new system will have a parallel connection from the DFEA to L1caltrack.

The Boston group has developed a stand-alone test board (DFEA Stand-Alone Tester or DSAT) which they used to test each board at Boston. Fermilab has a copy of the DSAT test setup. Five DSAT modules are available, one at BU, one at Fermilab, and three spares at BU.

During the accelerator shutdown in fall of 2004, two DFEA2 boards and a ninth octant card (CTOC) were installed on the platform. The inputs to the original DFEAs were split to provide identical inputs to the DFEA2s. This allowed comparison of the outputs of the new versus the original DFEA boards. The new boards were initially programmed with the same firmware as the existing DFEA cards, and it was confirmed that, in that configuration, the outputs of the old and new boards were identical. Then the DFEA2 boards were programmed with new singlet firmware, and it was confirmed that the DFEA2 output changed as expected. Therefore it has been established that one could return to the old firmware and reproduce the existing system. So the "do no harm" directive is satisfied.

In addition to the platform tests, two full crates of DFEA2 cards have undergone tests at Fermilab in DAB3. Although all boards are powered, not all communication paths have yet been tested, as discussed in more detail below.

Generation of the equations used to produce the VHDL is being done by Graham Wilson (Kansas). This task seems well in hand, with some improvements made from the procedure used previously. It takes him about one day to get a new version of VDHL. See the comment below concerning computing resources needed to produce the compiled firmware from the VDHL.

We commend the L1CTT group on the completeness of the documentation for the technical design of each of the system parts. We also commend the group for completing the hardware on a schedule that allows thorough tests of individual boards and substantial system tests.

A summary of the installation and commissioning plan was shown, and the L1CTT group feels that the installation is straightforwared. They have allowed 8 weeks for installation and 8 weeks for commissioning. The installation is estimated to take only two weeks, so their plan has substantial schedule contingency.

4 Comments and Concerns

In the discussion it became clear that the CPS cluster information is not being sent to the L1muon or L1caltrack systems. This requirement was part of the original specification of the RunIIb CTT upgrade, and this functionality should be retained. Adding this capability will require changes to the DFEA2 firmware, and the feasibility of this change must be confirmed. Providing the CPS information to the L1caltrack trigger will increase the latency of the trigger, since the CPS information is available somewhat later than the pure tracking information. How much later, and if the pipeline depth is enough to accommodate the delay, are important questions which are not yet answered.

The connections between the DFEA2s and L1muon/L1caltrack are new and have not been thoroughly tested. The L1 connection between the DFEA2 and the CTOC has been tested, but the L2 connections through the backplane between DFEA2 and CTOC, STOV, and STSX have not been tested. Also, the L2 information passed on to the L2 system has only been tested in VDHL functional simulation. Experience has shown that this kind of testing is not sufficient, as many bugs show up only when running the firmware on a real chip in the sytstem. The testing of board-to-board connections through the backplane (crucial for isolated track triggers) has also not been adequately tested.

Adequate software for online control and monitoring of the L1CTT system exists. However there was some indication that simplified tools would be helpful for shifters.

Compilation of the VDHL code to produce the downloadable HEX files takes between 1-2 hours per chip, depending on details of the system. There are 160 chips, so total compilation time could be as great as 320 hours. The firmware compilation could easily be parallelized, so if the collaboration needs speedy turnaround of firmware updates, adequate computing resources must be allocated.

Although an installation and commissioning plan was shown, a more detailed plan should be developed, with names and task durations attached to each task.

A detailed plan for hardware precommissioning and commissioning exists. The CTT group has allowed 8 weeks for installation and 8 weeks for commissioning. The installation is estimated to take only two weeks, but the time needed for physics commissioning is less certain. Efforts should be made to control and script the commissioning period as much as possible.

The upgraded L1CTT has not yet been incorporated into the trigger simulator, D0Ttrigsim, and therefore the hardware output has not been compared with the output of the trigger simulator. The

efficiency of the singlet firmware applied to actual data has not been compared to offline tracks, although the ability to so exists, since two DFEA2 boards are currently being read out through crate x13. These issues should be addressed, but we did not feel that they should impact the hardware installation.

We have some concern about the lack of a platform test with more than two DFEA2 modules in a crate. Though fully loaded DFEA crates have been exercised in the Combined Test Stand area on DAB3, many system problems become evident only after installation on the platform. The L1CTT group should consider adding additional DFEA2 modules, cables, and splitters to the crate on the platform so that any unforeseen system problems could be uncovered early. Even if it is not possible to fully cable up all of the DFEA2s, such a test could be informative. In the same vein, the new low voltage power distribution system should be exercised as much as possible, including and especially on the platform. The use of 48V bulk power regulated down to the required voltages is new for the lab, so experience with this type of power distribution is minimal. In particular, the DC-to-DC converters may generate noise which could affect the calorimeter. Although some tests have been done, a fully-loaded crate provides a more realistic test.

5 Questions from the Charge

In this section we specifically answer the questions posed in the Charge to the Committee. Questions posed to the committee are in **bold**.

Communication paths: Have the transmission of data and control signals been verified across all of the relevant communication paths (host/controller, controller/DFEA2, mixer/DFEA2, ...)

Not all communication paths are tested. Specific items that still need testing are detailed in the recommendations.

Are the bit error rates low enough for long-term operation?
Error rates have been demonstrated to be less than one part in 10^{16}.

Have new cables been tested?
Has connection and data integrity to TCC/TFW/L1Mu/L2/L3 been tested?
Has the connection to the Cal Track Match system been tested?
Some cables have been only DC tested. Since only the DFEA2 has been replaced, there should be no need to test connections to the Trigger framework or L3. Most connections to L2 also do not need to be tested. Still remaining to be tested are L2 connections to the CTOC, STOV and STSX, as well as the connections to L1muon and L1Caltrack.

System scaling: Has it been demonstrated that multiple DFEA2's in a crate (a full crate) operate without interference?
Is the measured power consumption compatible with specification?
Two full crates have been operated in the test stand in DAB3 with no problems occurring. But a fully-loaded crate has not been tested in full data-taking mode on the platform. Power consumption is well within specs.

Parallel chain tests: Have the parallel chain tests demonstrated that the hardware produces the expected results for doublets? singlets?
The expected results for doublets have been confirmed by comparing to the original DFEA outputs when the same firmware has been loaded in both new and old DFEAs. Comparison to the singlet firmware is qualitative, since the singlet firmware is not incorporated into Trigsim.

Software tools: Has software been written and exercised which
- download the hardware
- verifies the download
- monitors the operation for errors
- compares hardware output with emulation
- unpacks the CTT data which is written to the raw data chuck
- archives/tracks history of installed firmware
- monitors the system online
All of these are in hand except a method to track the version history of the firmware. Also, the output of the hardware when it is given specific test vectors has been tested, but there has not been a test with Trigsim.

Installation and maintenance plans: Have all the required safety approvals for installation been obtained, or are in the works?
Yes.

Is the installation infrastructure planned out, for example power, real estate, cabling, etc.
Some thought has been given to this, but the planning does not appear to be finalized.

What is the installation plan and who is going to do it?
We did not see a detailed installation plan, but the actual replacement of the crates and cabling is thought not to be a huge task. We did not see a plan for the physics commissioning, in particular, what questions must be answered concerning the performance of the CTT upgrade for physics, and who is going to do the necessary analysis?

How are boards going to be repaired in the long run? Are there adequate spares and test stands?
The ability to maintain the boards exists both at Boston and at Fermilab. There are adequate test stands, both at Boston and Fermilab, and there are sufficient spares.

Is it conceivable that changes might be required to hardware and/or firmware after installation and technical commissioning? How will the facilities and expertise for making these changes be available?
No hardware changes are anticipated at this time, but the ability to make changes exists both at Boston and at Fermilab. There will be changes to the firmware as experimental conditions change. Graham Wilson of the University of Kansas is committed to maintaining the equation generating machinery, and the ability to produce the firmware exists both at Fermilab and at Boston.

6 Recommendations

1. The L1CTT firmware developers should work with the L1caltrack group to specify and implement matching CPS bits with the track information sent to the L1caltrack/L1muon trigger systems. The impact of adding the CPS information on the DFEA2 latency should be determined.

2. Board-to-board communication over the backplane should be checked in the test stand, both electrically and with trigger algorithms using an appropriate set of test vectors.

3. Test the L2 communication from the DFEA2s boards to CTOC, STOV, and STSX. The data content as well as the connection should be tested. Communication between DFEA2 and L1caltrack and L1muon triggers should also be tested.

4. Additional LVDS cables should be ordered as soon as possible.

5. The DFEA2 crate currently on the platform should have as many additional DFEA2 modules installed as possible, even if they cannot all be cabled up. A fully-loaded crate on the platform might detect system noise that would not be present in the DAB3 test. Secondly, a fully loaded crate would more thoroughly test the power supplies in situ, perhaps shedding light on thermal as well as electrical issues. Thirdly, having a full crate of the DC-to-DC converters all running simultaneously might provide useful noise information to the calorimeter group.

6. Continue to develop monitoring and control software/documentation for shifters.

7. The machinery to compare L1CTT hardware output with the output from D0trigsim should be completed.

8. The data from the two DFEA2 boards on the platform should be compared to offline tracks to determine the efficiency of the singlet firmware.

9. All aspects of cabling and crate locations should be discussed with appropriate D0 personnel and finalized.

10. Develop a detailed script for installation, checkout, debugging, and physics commissioning of the L1CTT trigger. The script should include the tests to be performed as well as a short statement as to the decision paths to be followed should a given test fail. Names and durations should be attached to each of the tasks.

11. A great deal of documentation already exists. A central web page with links to all the relevant documents would be useful.

12. D0 management should ask Fermilab for PPD support for L1CTT for the life of the experiment.

13. Develop a system to ensure that the versions of firmware in use at any given time are clearly documented.

Committee Charge

All of the individual boards which make up the upgrade of the L1CTT have been shown to work on the test bench and meet their design specifications. The purpose of this review is to verify that all of the parts work in concert as a system so that there are no reservations about installing the system from the technical point of view. The scope of this review includes the online software as well as the hardware.

Particular points which should be covered include:

- Communication paths: Have the transmission of data and control signals been verified across all of the relevant communication paths (host/controller, controller/DFEA2, mixer/DFEA2, ...).
Are the bit error rates low enough for long-term operation?
Have new cables been tested?
Has connection and data integrity to TCC/TFW/L1Mu/L2/L3 been tested?
Has the connection to the Cal Track Match system been tested?

- System scaling: Has it been demonstrated that multiple DFEA2's in a crate (a full crate) operate without interference?
Is the measured power consumption compatible with specification?

- Parallel chain tests: Have the parallel chain tests demonstrated that the hardware produces the expected results for doublets? singlets?

- Software tools: Has software been written and exercised which
- download the hardware
- verifies the download
- monitors the operation for errors
- compares hardware output with emulation
- unpacks the CTT data which is written to the raw data chuck
- archives/tracks history of installed firmware
- monitors the system online

- Documentation: Is there adequate documentation for
- configuring and initializing the system
- interpreting errors flagged by the monitoring utilities
- specifying the data formats
- + documentation for each piece of hardware in the system

- Installation and maintenance plans:
- have all the required safety approvals for installation been obtained, or are in the works?
- is the installation infrastructure planned out, for example power, real estate, cabling, etc.?
- what is the installation plan and who is going to do it?
- how are boards going to be repaired in the long run? Are there adequate spares and test stands?
- is it conceivable that changes might be required to hardware and/or firmware after installation

and technical commissioning? How will the facilities and expertise for making these changes be available?

Agenda

Welcome and Overview, Lincoln (10 min) (slides)
DFEA2 (Hazen, 30 minutes) (slides)
DFE Testing (Khalatyan, 30 minutes) (slides)
DFE at Fermilab + Installation Plan (Gruenendahl, 60 minutes) (slides)
Tour of equipment (30 minutes)
Working Lunch, Committee only (2 hours)
CTT Meets with Committee (until it's over)